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Claims

[c1] A method of forming a semiconductor device in a semiconductor substrate comprising the steps of:
etching a trench having trench axes parallel to <100> directions of said substrate, said trench having a square cross section in a lower portion and an octagonal cross section in an upper portion;
forming a liner layer of liner material on interior walls of said trench in said upper portion, whereby said liner layer has a first thickness on {100} surfaces of said interior walls;
etching said liner layer selective to the substrate, whereby said liner layer remains on said {100} surfaces and corners of said trench are exposed;
etching said interior walls selective to said liner layer, whereby said octagonal cross section is converted to a rectangular cross section having a trench wall width between trench corners.

[c2] A method according to claim 1, in which said substrate is silicon and said liner material is selected from the group comprising $Si_{1-x}Ge_x$ and $Si_{1-x-y}Ge_xC_y$, further comprising a step of:

stripping said liner material from said interior walls after said step of etching said interior walls selective to said liner material.

[c3] A method according to claim 1, in which said substrate is silicon and said liner material is selected from the group comprising $Si_{1-x}Ge_x$ and $Si_{1-x-y}Ge_xC_y$; and further comprising a step of:
epitaxially growing silicon on said interior walls and on said liner material after said step of etching said interior walls selective to said liner material.

[c4] A method according to claim 1, in which said substrate is silicon and said liner material is selected from the group comprising $Si_{1-x}Ge_x$ and $Si_{1-x-y}Ge_xC_y$; and further comprising a step of:
epitaxially growing silicon on said interior walls and on said liner material after said step of etching said interior walls selective to said liner material.

[c5] A method according to claim 2, in which said first thickness is reduced to a second thickness after said step of etching said liner material selective to the substrate, said second thickness being such that remaining liner material protects {100} surfaces of said interior walls during said step of etching said interior walls selective to said liner material.

[c6] A method according to claim 5, in which said step of etching said interior walls selective to said liner material is performed with an etchant including a compound from the group consisting of ammonia, tetramethyl ammonium hydroxide and a mixture of nitric and hydrofluoric acid.

[c7] A method according to claim 4, in which said first thickness is reduced to a second thickness after said step of etching said liner material selective to the substrate, said second thickness being such that remaining liner material protects {100} surfaces of said interior walls during said step of etching said interior walls selective to said liner material.

[c8] A method according to claim 7, in which said step of etching said interior walls selective to said liner material is performed with an etchant including a compound from the group consisting of ammonia, tetramethyl ammonium hydroxide and a mixture of nitric and hydrofluoric acid.

[c9] A method according to claim 3, in which said first thickness is reduced to a second thickness after said step of etching said liner material selective to the substrate, said second thickness being such that remaining liner mate-

rial protects {100} surfaces of said interior walls during said step of etching said interior walls selective to liner material.

[c10] A method according to claim 9, in which said first thickness is reduced to a second thickness after said step of etching said liner material selective to the substrate, said second thickness being such that remaining liner material protects {100} surfaces of said interior walls during said step of etching said interior walls selective to said liner material.

[c11] A method according to claim 2, in which said step of depositing a liner material is performed with UHVCVD.

[c12] A memory cell in a semiconductor substrate comprising:
a trench having trench axes parallel to <100> directions of said substrate, said trench having a square cross section in a lower portion and a capacitor in said lower portion, said square cross section in said lower portion having diagonals parallel with said <100> directions of said silicon substrate;
at least one vertical transistor formed in said upper portion of said trench said vertical transistor having a channel in a first trench wall surface of said upper portion of said substrate extending between a pair of corners formed by etching exposed substrate selective to a tem-

porary layer selected from the group comprising $Si_{1-x}Ge_x$ and $Si_{1-x-y}Ge_xC_y$; on said trench wall surface.

[c13] A memory cell according to claim 12, in which:
said first trench wall surface is a {100} surface.

[c14] A trench memory cell according to claim 12, in which:
said pair of corners are formed by etching with an etchant including a compound from the group consisting of ammonia, tetramethyl ammonium hydroxide and a mixture of nitric and hydrofluoric.

[c15] A memory cell in a semiconductor substrate comprising:
a trench having trench axes parallel to <100> directions of said substrate, said trench having a square cross section in a lower portion and a capacitor in said lower portion, said square cross section in said lower portion having diagonals parallel with said <100> directions of said substrate;
at least one vertical transistor formed in said upper portion of said trench said vertical transistor having a channel in a layer of SiGe adjacent to a first trench wall surface of said upper portion of said substrate extending between a pair of corners formed by etching exposed substrate selective to said layer of SiGe on said trench wall surface.

[c16] A memory cell according to claim 15, in which:
said first trench wall surface is a {100} plane.

[c17] A memory cell according to claim 16, in which:
said pair of corners are formed by etching with an etchant including a compound from the group consisting of ammonia, tetramethyl ammonium hydroxide and a mixture of nitric and hydrofluoric acid.

[c18] A memory cell according to claim 15, further comprising a gate oxide thermally grown on an epitaxial layer of silicon formed on both said layer of SiGe and on exposed trench walls.

[c19] A memory cell according to claim 18, in which:
said first trench wall surface is a {100} plane.

[c20] A memory cell according to claim 19, in which:
said pair of corners are formed by etching with an etchant including a compound from the group consisting of ammonia, tetramethyl ammonium hydroxide and a mixture of nitric and hydrofluoric acid.